ISLA11xP50 Output Data Timing and Synchronization

Overview

Capturing data from the ISLA11xP50 ADC is easily accomplished with current FPGA technology. The source-synchronous LVDS interface provides DDR output data at up to 500MHz with a 250MHz clock. The clock and data are aligned within ±250ps providing a wide guaranteed data-valid region of 1.5ns over the full range of process, voltage and temperature at 500MSPS operation.

Internally the input clock is immediately divided by two in order to clock the two ADC cores at half the output sample rate. Even though the 500MSPS output data stream is generated by two interleaved ADC cores, the output data is always delivered from a single ISLA11xP50 in a known sequence. Multiple ADCs with aligned input clock edges may not have aligned output clock edges due to the divide-by-two's uncertain output phase. The CLKOUTP signal can be high or low at the rising edge of the input clock unless specifically forced to a known state.

The ISLA11xP50 includes synchronization features making it easier to design systems requiring simultaneous sampling or further interleaved sampling. Synchronization may be as simple as using a single ADC output data clock or the CLKDIVRST pins to force synchronization. More complex approaches may use the PHASE_SLIP register to adjust timing. The best method will depend on many factors including the timing margin, the FPGA family, the FPGA design tools and printed circuit board (PCB) constraints. At 500MSPS operation the CLKDIVRSTP setup and hold timing may be challenging for some designs. These timing requirements may be effectively relaxed by gating the ADC input clock to provide additional margin.

This document is intended to provide basic guidance on the ISLA11xP50's output timing and synchronization methods.

Output Timing

The ISLA11xP50 input clock and data propagate through the ISLA11xP50 with a similar delay path in order to relax data capture timing requirements. The ADC output DATA will transition from one sample to the next within ±250ps of the CLKOUTP signal; leaving a wide data-valid window of 1.5ns at 500MSPS. CLKOUTP will be delayed from CLKP by 2.6ns to 3.3ns at 1.8V and +25°C as shown in Figure 1 or by 2.0ns to 3.6ns over the entire recommended operating range of 1.7V to 1.9V from -40°C to +85°C.

Internal Operation

The interleaved operation of the ISLA11xP50 requires the 500MHz input clock to be divided by two so that each core samples at 250MSPS. Figure 2 shows a conceptual view of the ADCs internal clock circuitry. The clock divider normally comes out of power-on reset in a random state so the output clock phase (CLK_A, CLK_B in Figure 2) is indeterminate. In normal operation with a single ADC the unknown clock phase does not matter and the output sample order is always correct. This may not be the case when synchronizing multiple ADCs. The uncertainty in CLKOUTP phase means the CLKOUTP rising edges may not be aligned across multiple ADCs driven by the same clock source. This possible phase difference as shown in Figure 3 can lead to an unexpected difference in sample time and sequence in the captured data.

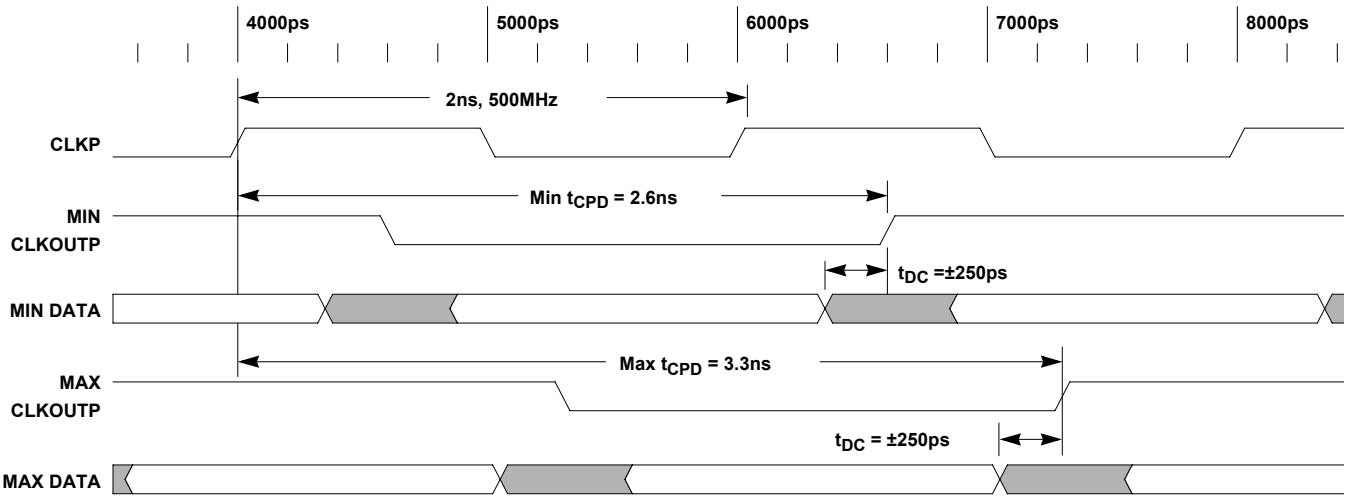


FIGURE 1. 1.8V AT +25°C ADC OUTPUT TIMING

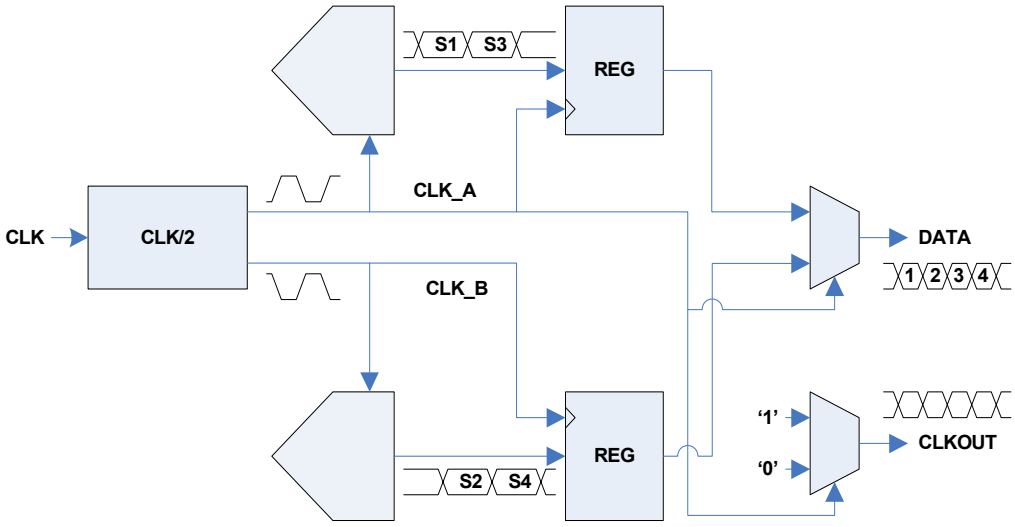
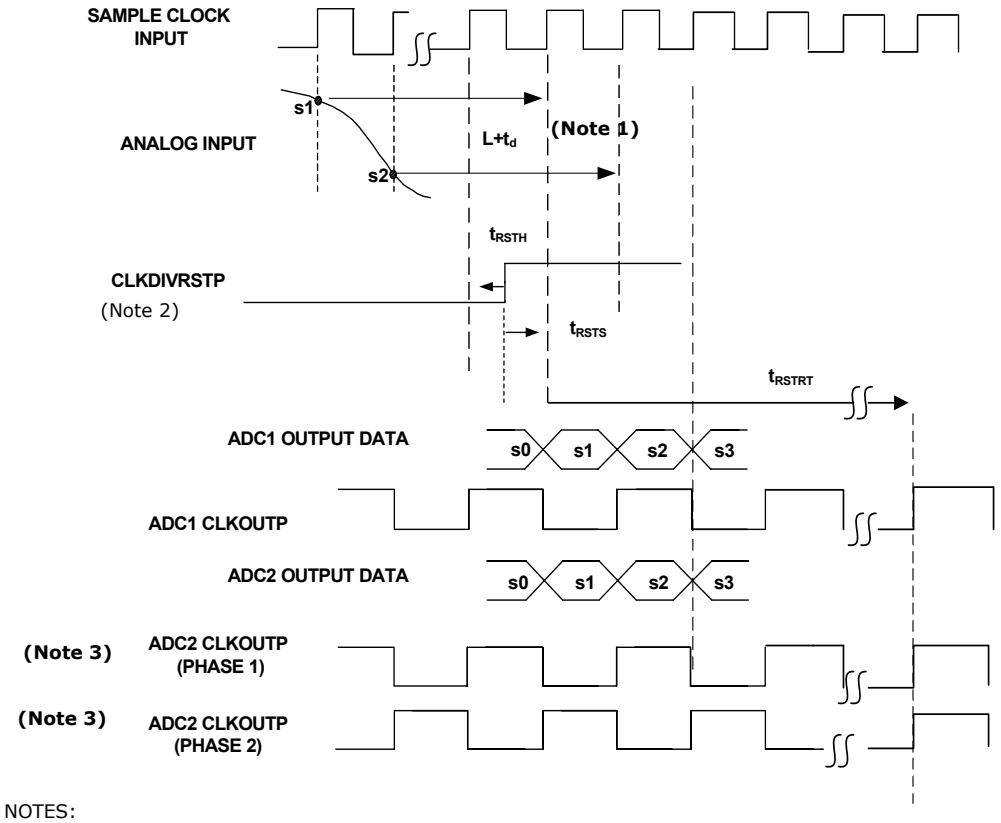


FIGURE 2. ADC INTERNAL DATA CLOCKING



NOTES:

1. Delay equals fixed pipeline latency (L cycles) plus fixed analog propagation delay td
2. CLKDIVRSTP setup and hold times are with respect to input sample clock rising edge. CLKDIVRSTN is not shown, but must be driven, and is the compliment of CLKDIVRSTP.
3. Either Output Clock Phase (phase 1 or phase 2) equally likely prior to synchronization.

FIGURE 3. MULTIPLE ADC CLKOUT PHASE UNCERTAINTY

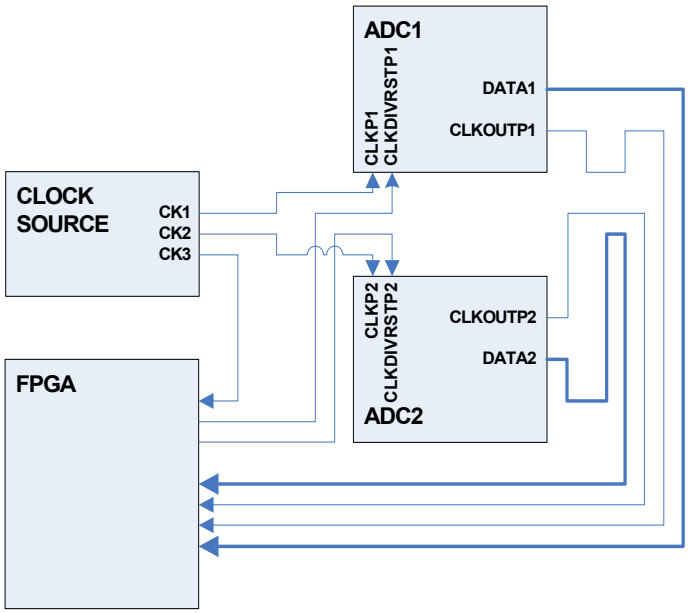


FIGURE 4. MULTIPLE ADC SYNCHRONIZATION CIRCUITRY

Synchronization

The ISLA11xP50 provides two mechanisms to control the output clock phase:

1. The CLKDIVRSTP pins offer the simplest method to synchronize multiple ADCs. When CLKDIVRSTP is set high within the datasheet setup and hold times the CLKOUTP signal will always be forced to a known phase. Routing CLKP and CLKDIVRSTP to multiple ADCs with equal PCB delays allows all ADCs to be simultaneously set to the same sample phase. Assertion of CLKDIVRSTP may cause the internal DLL to lose lock for up to 52µs. Valid data may be captured after this 52µs period. This process must be completed after each power cycle or ADC reset.
2. The PHASE_SLIP register (0x71) can be written to effectively invert the CLKOUTP signal. The User Test Mode allows a pair of known values to be output but using these values to identify the clock phase relationship requires more FPGA code than using CLKDIVRSTP. After synchronization with CLKDIVRSTP the PHASE_SLIP register can be used to delay the output data to further interleave multiple ADCs.

If relaxed setup and hold times are required for CLKDIVRSTP the input clock can be gated off, CLKDIVRSTP set high then the clock re-enabled. Glitchless clock gating circuitry must be used to assure reliable operation.

Figure 4 illustrates the connections necessary to synchronize two ADCs with CLKDIVRSTP. Note that any mismatch in the CLKP and CLKDIVRSTP traces must be accounted for in the timing budget. Additional ADCs may be synchronized by extending the circuitry in Figure 4 for as many ADCs as necessary.

Multiple ADC Timing Margin

Device-to-device timing becomes important for two reasons when multiple devices are to be synchronized.

1. In some cases it may be possible to synchronize multiple ADCs by only using a single clock. This eliminates the clock phase uncertainty since all the data is captured by a single clock. The downside is reduced timing margin since each ADC will have slightly different timing. The dt_{CPD} specification can be used to quantify this uncertainty.
2. The FPGA must be able to manage the difference in clock delay through the ADCs in order to correctly capture the data. Managing timing where the clock may slip one or more cycles across the ADCs is simplified by current FPGA technology's ability to automatically align input data streams with a known pattern. Design examples are available from Xilinx (XAPP1064) and Altera (AN236). Search their web pages for 'source-synchronous ddr' to find more examples.

Each ADCs output data will transition within ±250ps of the CLKOUTP signal. CLKOUTP will be delayed from CLKP by 2.6ns to 3.3ns at 1.8V and +25°C as shown in Figure 5. When more than one ADCs output data is to be captured using a single CLKOUTP signal the valid data window is a minimum of 800ps (1.8V, +25°C).

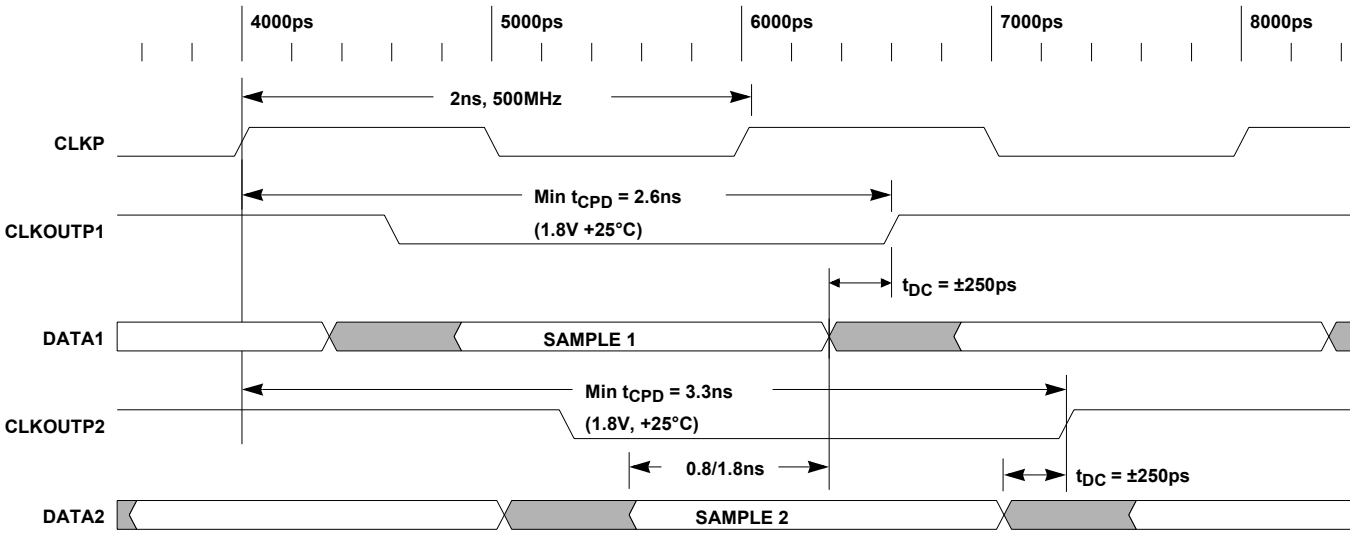


FIGURE 5. 1.8V AT +25°C MULTIPLE ADC TIMING SKEW

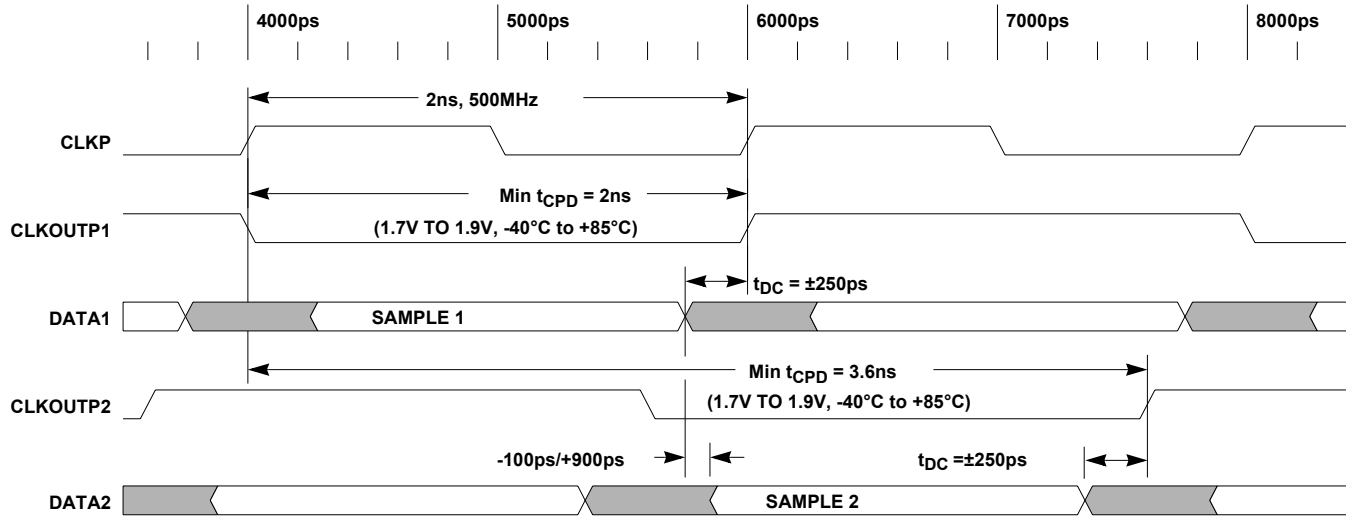


FIGURE 6. 1.7V TO 1.9V AT -40°C TO +85°C MULTIPLE ADC TIMING SKEW

If the ADCs are at the opposite extremes of voltage and temperature (i.e. ADC1 sees 1.9V @ -40°C and ADC2 sees 1.7V at +85°C) the timing will be at the worst possible specified skew as shown in Figure 6. In this case, operation at 500MHz will most likely result in negative timing margin. This means a single ADCs output clock cannot be used to capture data from multiple ADCs without adjusting the FPGA capture for proper data sequence. Even when using each ADCs output clock the FPGA may have to tolerate a possible one cycle clock slip between devices.

Relative Output Clock Delay Matching (dt_{CPD})

A more realistic design will operate all the synchronized ADCs at the same voltage and temperature. This is the condition covered by the dt_{CPD} specification. This specification says CLKOUTP from all devices at the same voltage and temperature will fall with ±450ps of the nominal timing (CLKOUT_NOM) of CLKOUTP from any other ADC as shown in Figure 7. This means that both devices' CLKOUTP will be within a 900ps window bounded by the t_{CPD} specification over the full voltage and temperature range. Either device can lead or lag the nominal by up to 450ps so the FPGA must be able to manage up to a ±900ps delta between ADCs even when they are synchronized with CLKDIVRSTP. The ISLA11xP50's fixed pattern capability works with the FPGA's DDR capture circuitry to automatically enable robust data capture over a range of more than one clock cycle as described in application notes from Xilinx (XAPP1064) and Altera (AN236). The minimum valid data window for this condition is 600ps. The variation in the ±250ps data transition relative to the output clock is dominated by matching and is not correlated to the overall input to output clock delay.

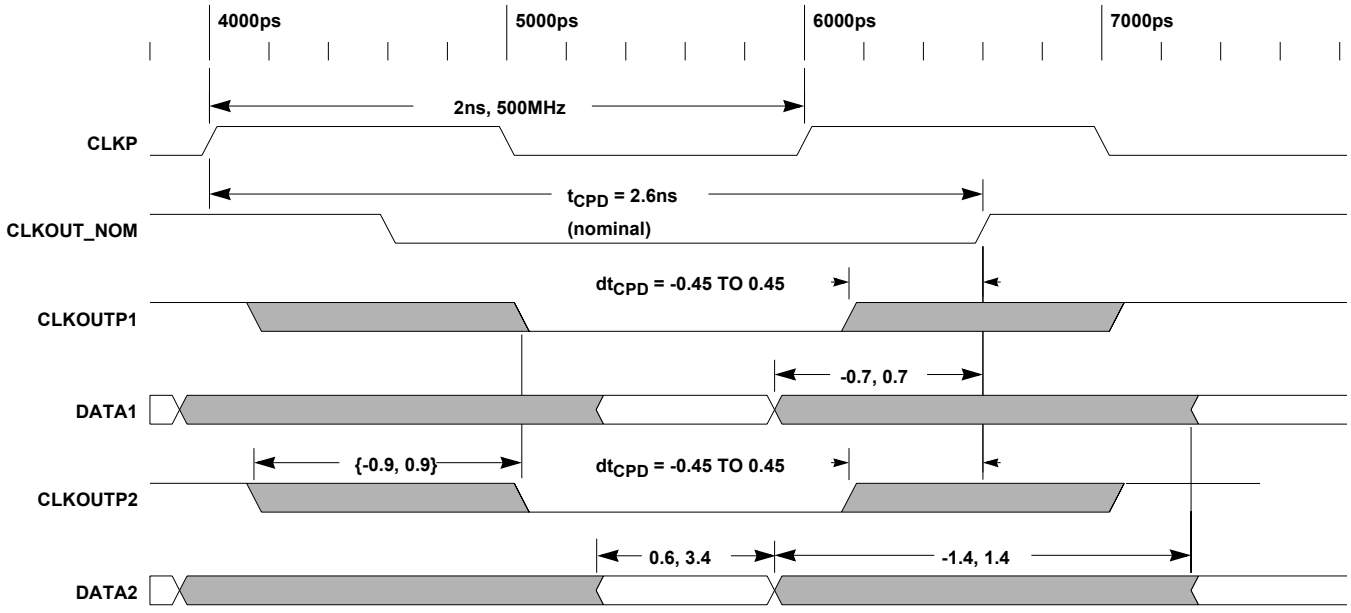


FIGURE 7. PART-TO-PART TIMING FOR ADCS, EQUAL VOLTAGE AND TEMPERATURE

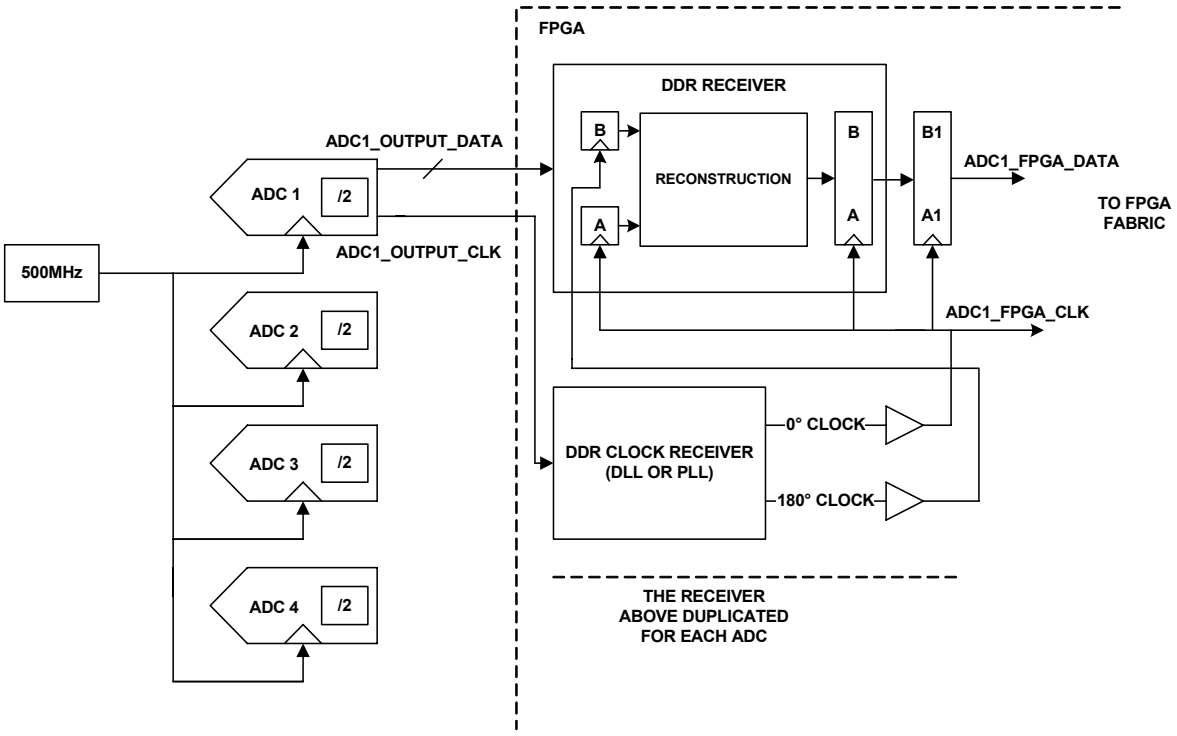


FIGURE 8. FPGA DATA CAPTURE

FPGA Data Capture

One possible FPGA data capture implementation is shown in Figure 8. The DDR clock receiver is used to generate the 180° DDR clock. The incoming data and clock are aligned within ±250ps from the ISLA11xP50 so the FPGA must also shift the clock relative to the data for optimum data capture. The data from any one ADC may be offset up to 900ps from any other ADC when they operate at the same voltage and temperature. Care must be taken to provide sufficient timing margin since the 900ps offset can be in either direction possibly affecting the DDR receiver's setup and hold time. Current FPGA data capture circuitry includes features that can simplify recovery of source synchronous DDR data streams.

Note

CLKP, CLKOUTP and CLKDIVRSTP all refer to the positive LVDS signals which also include the CLKN, CLKOUTN and CLKDIVRSTN complement signals. All LVDS signals must be routed as differential pairs. All timing numbers are for LVDS signals and are copied from the datasheet for convenience. The datasheet timing specifications take precedence in all cases since this document does not guarantee performance limits.